COURSE TITLE : DIGITAL COMPUTER PRINCIPLES LAB

COURSE CODE : 3138

COURSE CATEGORY : B

PERIODS/WEEK : 5

PERIODS/SEMESTER : 75

CREDITS : 3

Course General Outcomes:

The student should be able to do the experiments from the following topics on completion of corresponding topic

1.0 To implement basic logic gates

- 1.0.1 Implement logic gates using basic components
- 1.0.2 Verify the Logic behaviour of various IC gates: 7408, 7432, 7404, 7400, 7402, 7486)
- 1.0.3 Implement basic gates using Universal Gates (NAND & NOR)
- 1.0.4 Simplification of Boolean Functions SOP & POS forms (Demonstrates the relationship between a Boolean Function and the corresponding logic diagram – using Map reduction method)

Eg: Plot the following Boolean function in a Map as well as implement in a logic diagram

F = A'D + BD + B'C + AB'D

2.0 To design and Implement Combinational Circuits

- 2.0.1 Implement the following Combinational Circuits (Design, construct, and test combinational logic circuit that generates parity bit from four message bits)
- 2.0.2 Design a combinational circuit that converts a Gray code to binary, Decoder for a binary digit to BCD, and a seven segment indicator
- 2.0.3 Design, construct, and test a half-adder & a full-adder Implement using Basic gates and Universal gates
- 2.0.4 Implement a circuit using a four-bit binary parallel adder (IC 7483) implement Adder-Subtractor, and a Magnitude Comparator)

3.0 To demonstrate synchronous sequential logic

- 3.0.1 Construct, Test, and investigate the operation of SR Latch, D Latch, Master-Slave Flip-Flop, Edge-Triggered Flip-Flop, IC Flip-Flops(using IC 7476, and 7474)
- 3.0.2 Sequential Circuits (Design, construct, and test Up-Down counter with Enable)
- 3.0.3 Design, construct, and test a counter that goes through a sequence of binary states (User controlled counting pattern)
- 3.0.4 Construct, and test Ripple Counter, Synchronous counter, Decimal Counter
- 3.0.5 Setup a Binary counter with Parallel Load (use IC 74161))
- 3.0.6 Study the operation of Shift Registers (Investigate the operation of Shift Registers, Ring Counter, Feedback Shift Register, Bidirectional Shift register, Bidirectional Shift Register with Parallel Load)