

TED (15) - 3131

(REVISION - 2015)

Reg. No	 	 	
Signature	 ***********	 	

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY — OCTOBER, 2016

COMPUTER ARCHITECTURE

(Common for CT and CM)

[Time: 3 hours

(Maximum marks: 100)

PART - A

(Maximum marks: 10)

Marks

- I Answer the following questions in one or two sentences. Each question carries 2 marks.
 - 1. Define bus.
 - 2. Define RAID.
 - 3. List any two control registers.
 - 4. Define MIMD.
 - 5. Define fetch overlap.

 $(5 \times 2 = 10)$

PART — B

(Maximum marks: 30)

- II Answer any five of the following questions. Each question carries 6 marks.
 - 1. Illustrate the interaction between the top level computer components with the help of a neat sketch.
 - 2. List and explain I/O module functions.
 - 3. Explain instruction cycle micro-operations.
 - 4. Write short note on parallel processing.
 - 5. List and explain different types of ROM.
 - 6. Explain physical characteristics of a magnetic disk system.
 - 7. Describe micro-operations.

 $(5 \times 6 = 30)$



Marks

PART — C

(Maximum marks: 60)

(Answer one full question from each unit. Each full question carries 15 marks.)

UNIT -- I

		UNII — I	
III	(a)	Explain multiple bus hierarchy with diagram.	8
	(b)	Describe memory hierarchy with the help of a neat sketch.	7
		OR	
IV	(a)	Explain Elements of bus design.	8
	(b)	Describe advanced DRAM types.	. 7
		Unit — II	
V	(a)	Explain I/O module structure with neat structure.	8
	(b)	Explain magnetic disk read and write mechanism.	7
		OR	
VI	(a)	Compare RAID levels.	8
	(b)	Explain DMA function.	7
		Unit — III	
VII	(a)	Describe processor organization with the help of internal structure diagram.	7
	(b)	Explain data flow in instruction cycle.	8
		OR	
VIII	(a)	Explain control and status register.	8
	(b)	Explain instruction pipelining.	7
		Unit — IV	
IX	(a)	Explain interrupt cycle micro-operations.	7
	(b)	List and explain Flynn's classification of parallel processing systems.	8
		OR	
X	(a)	Describe microprogrammed control unit.	7
	(b)	Draw the general parallel processor organizations and explain.	8