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# DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE - OCTOBER, 2018 

## DJGITAL COMPUTER PRINCIPLES

[Time : 3 hours
(Maximum marks : 100)

PART - A
(Maximum marks : 10)

I Answer all questions in one or two sentences. Each question carries 2 marks.

1. Define base of a number system.
2. What is parity bit ?
3. Define Encoder.
4. Define latch.
5. What is PAL?

## PART - B

(Maximum marks : 30)
II Answer any five of the following questions. Each question carries 6 marks.

1. Write short notes on BCD codes.
2. State and prove De-Morgan's theorem.
3. Realize EX-OR, OR gates using NAND gate.
4. Expand $\mathrm{A}^{\prime}+\mathrm{B}^{\prime}$ to minterms and maxterms.
5. Explain the working of a D-flipflop.
6. Differentiate synchronous and asynchronous sequential circuits.
7. Explain how memory decoding is performed.

PART - C
(Maximum marks : 60)
(Answer one full question from each unit. Each full question carries 15 marks.)

## Unit - I

III (a) Convert the following :
(i) $(11011.101)_{2}$ to Decimal
(ii) (BFA6) ${ }_{16}$ to binary
(iii) (756.603) $\mathbf{8}_{8}$ to hexa decimal
(b) Reduce and draw the logic diagram for the Boolean expression $F=A(B+C)+B^{\prime}(B+D)$

Or
IV (a) Explain basic gates with truth table and logic diagram.
(b) Explain the procedure of obtaining an equivalent gray code for a binary code with example.
Unit - II
$V$ (a) Simplify the Boolean function $F(w, x, y, z)=\sum \mathrm{m}(1,3,7,11,15)$ which has the don't-care conditions $d(w, x, y, z)=(0,2,5)$.
(b) Design a half adder with truth table and logic diagram.

## Or

VI (a) Design a decimal Adder with truth table and logic diagram.
(b) Write short notes on SOP and POS forms.

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VII Explain about different types of shift registers.
Or
VIII (a) Explain the working of a JK-Flipflop with truth table and diagram.
(b) Design a 3 bit up counter.
UNIT - IV

IX (a) Explain the specifications of a DAC. 8
(b) Explain construction of memory cell with logic diagram. 7

## Or

X (a) Explain the working of programmable logic array with an example. 9
(b) Explain a R-2R ladder DAC. 6

